REMARKS

In the Office Action, the Examiner objected to claims 19-37, 42 and 43. Claim 42 has been amended, as has the Specification. Upon entry of the Amendments, claims 19-37, 42 and 43 will remain pending in the present patent application. Reconsideration and allowance of all pending claims are requested.

Objections to the Specification

The Examiner objected to the Specification due to the absence of mention of the parent patent of which this application is a divisional. By the present response, the passage suggested by the Examiner has been added.

Rejections Under 35 U.S.C. § 102

Claims 19, 24, 27, 42 and 43 were rejected under 35 U.S.C. § 102(b) as being anticipated by Jaskie et al., U.S. Patent No. 5,606,215. Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration.

Claim 19 recites a method for forming a field emitter device. In accordance with the method, a first insulating layer is formed on a substrate, and a conducting gate layer is formed on the insulating layer. A field emitter tip is then formed on the substrate adjacent to the first insulating layer and the conducting layer. Finally, a second insulating layer is formed on at least one side surface of the conducting gate layer adjacent to the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

The Examiner indicated that similar components were found in the Jaskie et al. arrangement. However, Jaskie et al. do not anticipate the method of claim 19 for at least the reason set forth below.

The arrangement of Jaskie et al. relies upon a combination of a resistive layer and an optional dielectric layer to dissipate charge and avoid arcing. In particular, the entire disclosure of Jaskie et al. focuses on the provision of a resistive layer 18, shown in the single figure of the reference, that dissipates charge. The dielectric layer 19 is, indeed, an optional layer, not even required by Jaskie et al. for performing the desired charge dissipation. As described in detail in the reference:

> Furthermore, an optional dielectric layer 19 may be applied over resistive layer 18 to further increase the resistance between gate 17 and emitter 14. *However, it should be noted that insulators develop a charge buildup that eventually results in a destructive breakdown arc between the insulator and emitter 14.* Consequently, the thickness of layer 19 must be sufficiently thin to maintain a high resistance path between the emitter 14 and gate 17. This high resistance path allows charge buildup to be dissipated through the resistive path thereby preventing a destructive arc.

Jaskie et al., column 2, line 50 – column 3, line 2. (Emphasis added).

Clearly, Jaskie et al. do not favor the use of an insulator to avoid arcing between a field emitter tip and a conducting gate layer. Rather, the reference actually *teaches away* from such solutions.

The approach of Jaskie et al. is counter to that recited in claim 19. Accordingly to claim 19, and as made clear throughout the present application, and in particular as illustrated in FIG. 2, the insulating layer is formed "on at least one side surface of the conducting gate layer adjacent to the field emitter tip." The optional dielectric layer 19 of Jaskie et al. is not formed on a surface of the conducting gate layer, but is formed on the resistive layer 18. It is this resistive layer that dissipates charge and avoids arcing.

Indeed, from the passage quoted above, one skilled in the art might conclude two things. First, a dielectric layer is not required, and might even be deleterious to the

operation of the device, in fact promoting arcing, particularly if no charge dissipating resistive layer is present, or the dielectric layer is too insulative. Secondly, one might conclude that the resistive layer 18 of Jaskie et al. is actually preferable to and favored over the provision of an insulating layer, and certainly over the provision of an insulating layer alone.

Accordingly, Jaskie et al. do not teach an arrangement that can support a *prima facie* case of anticipation of claim 19. Accordingly, claim 19 and the claims depending therefrom are believed to be clearly patentable over Jaskie et al. as well as other prior art of record.

Independent claim 42 was similarly rejected as anticipated by Jaskie et al. Claim 42 has been amended by this Response. The amendment adds that the arc prevention layer recited in the claim substantially covers the conducting gate layer adjacent to the field emitter tip. Such an arrangement is not taught by Jaskie et al.

On the contrary, as can be clearly seen in the single figure of Jaskie et al., a portion of the gate layer 17 actually extends over the opening 22 in which the emitter 14 is positioned. Indeed, this extension is noted by Jaskie et al. as "inside surface 23." It is over this surface that the resistive layer 18 is applied. However, the gate layer 17 clearly protrudes beyond the insulator layer 12. Thus, even if the resistive layer 18 were considered to be an arc prevention layer, this layer does not substantially cover the conducting gate layer adjacent to the field emitter tip.

Because Jaskie et al. do not teach an arc prevention layer substantially covering the conducting gate layer adjacent to the field emitter tip, the reference cannot anticipate claim 42. Moreover, because claim 43 recites that this arc prevention layer is a semiconductor material, the resistive layer 18 of Jaskie et al. cannot qualify to anticipate claim 43. Even if the dielectric layer 19 is considered, this layer also does not

substantially cover the conducting gate layer adjacent to the field emitter tip in the embodiment of Jaskie et al.

The Applicants therefore respectfully submit that independent claims 19 and 42 are allowable. Claims 24, 27 and 43 depend directly or indirectly on claims 19 and 42. Accordingly, Applicants submit that the claims 24, 27 and 43 are allowable by virtue of their dependency from the allowable base claims, as well as for the subject matter they separately recite. Thus, it is respectfully requested that the rejections of claims 19, 24, 27, 42 and 43 under 35 U.S.C. §102(b) be withdrawn.

Rejections Under 35 U.S.C. § 103

Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaskie et al. in view of Doan et al., U.S. Patent No. 5,259,799. Claims 22, 23, 25, 26, 28-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaskie et al. in view of Tjaden et al., U.S. Patent No. 6,190,223. Claim 33 and 35 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaskie et al. in view of Den et al., U.S. Patent No. 6,628,053.

The secondary references do not obviate the deficiencies of Jaskie et al. as regards claim 19. Applicants respectfully submit that claims 20, 22, 23, 25, 26, 28-34, 33 and 35 are allowable at least in view of their dependency on base claim 19, in addition to the subject matter they separately recite. Thus, it is respectfully requested that the rejections of claims 20, 22, 23, 25, 26, 28-34, 33 and 35 under 35 U.S.C. §103(a) be withdrawn.

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully request allowance of the pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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